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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,759	03/26/2004	Jiong-Ping Lu	TI 37793	9075

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EXAMINER

LUU, CHUONG A

ART UNIT PAPER NUMBER

2818

DATE MAILED: 11/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/810,759

Applicant(s)

LU ET AL.

Examiner

Chuong A. Luu

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 9/15/2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Response to Arguments***

Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

## **PRIOR ART REJECTIONS**

### **Statutory Basis**

#### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

### **The Rejections**

Claims 1-3, 7 and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim (U.S. 6,864,178 B1).

Kim discloses a MOS transistor with

**(1)** forming a polysilicon gate electrode (25) over a substrate (21);

forming source/drain regions (23) in said substrate (21) proximate said polysilicon gate electrode (25);

forming a blocking layer (27) over said source/drain regions (23) in a step, said blocking layer comprising a metal silicide (see Figure 2c);

siliciding said polysilicon gate electrode to form a silicided gate electrode (31) (see column 2, lines 31-67; column 3, lines 1-8. Figures 2a-2e);

(2) wherein said forming a blocking layer occurs prior to said siliciding said polysilicon gate electrode (see Figures 2a-2e);

(3) wherein said blocking layer is a silicided source/drain contact region (see Figures 2a-2c);

(7) further including forming a protective layer (29) over said polysilicon gate electrode (25) prior to said forming a blocking layer over said source/drain regions (23) (see column 2, lines 42-46);

(9) wherein siliciding said polysilicon gate electrode to form a silicided gate electrode includes fully siliciding said polysilicon gate electrode to form a fully silicided gate electrode (see column 3, lines 1-8. Figures 2a-2e).

## **PRIOR ART REJECTIONS**

### **Statutory Basis**

#### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

### **The Rejections**

Claims 4-6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (U.S. 6,864,178 B1) in view of Wieczorek et al. (U.S. 6,620,718 B1).

Kim teaches everything except for wherein said blocking layer comprises a cobalt silicide and said silicided gate electrode comprises a nickel silicide; wherein said blocking layer has a thickness ranging from about 10 nm to about 35 nm and silicon nitride. However, Wieczorek discloses a semiconductor device with **(4)** wherein said silicided gate electrode (see column 6, lines 6-15) comprises a different metal silicide than said blocking layer (see column 4, lines 50-55); **(5)** wherein said blocking layer comprises a cobalt silicide (see column 4, lines 50-55) and said silicided gate electrode comprises a nickel silicide (see column 6, lines 6-15); **(6)** wherein said blocking layer has a thickness ranging from about 15nm to about 75nm (10 nm to about 35 nm) (see column 5, lines 3-5); **(8)** wherein said protective layer is a silicon nitride protective layer (see column 4, lines 13-17). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify and select the specifically materials for blocking layer comprises a cobalt silicide and said silicided gate electrode comprises a nickel silicide; the thickness of the blocking layer from about 10 nm to about 35 nm of Kim's device (in accordance with the teaching of Wieczorek) within the range as claimed for the purpose of providing for reduced power consumption and increase operational speed, and it also has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves

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only routine skill in the art and it is noted that the applicant does not disclose criticality in the ranges claimed. In re Aller, 105 USPQ 233 (see MPEP j 2144.05).

Claims 10-12, 16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (U.S. 6,864,178 B1) in view of Pelella et al. (U.S. 6,830,987 B1).

Wieczorek discloses a semiconductor device with

**(10)** forming a polysilicon gate electrode (25) over a substrate (21);

forming source/drain regions (23) in said substrate (21) proximate said polysilicon gate electrode (25);

forming a blocking layer (27) over said source/drain regions (23) in a step, said blocking layer comprising a metal silicide (see Figure 2c);

siliciding said polysilicon gate electrode to form a silicided gate electrode (31) (see column 2, lines 31-67; column 3, lines 1-8. Figures 2a-2e);

**(11)** wherein said forming a blocking layer occurs prior to said siliciding said polysilicon gate electrode (see Figures 2a-2e);

**(12)** wherein said blocking layer is a silicided source/drain contact region (see Figures 2a-2c);

**(16)** further including forming a protective layer (29) over said polysilicon gate electrode (25) prior to said forming a blocking layer over said source/drain regions (23) (see column 2, lines 42-46);

**(18)** wherein siliciding said polysilicon gate electrode to form a silicided gate electrode includes fully siliciding said polysilicon gate electrode to form a fully silicided gate electrode (see column 3, lines 1-8. Figures 2a-2e).

Kim teaches the above outlined features except for forming interconnects within dielectric layers located over said substrate for electrically contacting said semiconductor devices. However, Pelella discloses a semiconductor device with **(10)**... forming interconnects within dielectric layers located over said substrate for electrically contacting said semiconductor devices (see Figure 5). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the MOS transistor of Kim (accordance with the teaching of Pelella). Doing so would facilitate the manufacture of the semiconductor MOS transistor and increase the speed of the semiconductor device.

Claims 13-15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (U.S. 6,864,178 B1) in view of Pelella et al. (U.S. 6,830,987 B1) and further in view of Wieczorek et al. (U.S. 6,620,718 B1).

Kim and Pelella teach the above outlined features except for selecting different materials for the silicided gate electrode and the blocking layer; wherein said protective layer is a silicon nitride protective layer and the blocking layer has a specific thickness ranging from about 10 nm to about 35 nm. Furthermore, Wieczorek discloses a semiconductor device **(13)** wherein said silicided gate electrode (see column 6, lines 6-15) comprises a different metal silicide than said blocking layer (see column 4, lines 50-

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55); **(14)** wherein said blocking layer comprises a cobalt silicide (see column 4, lines 50-55) and said silicided gate electrode comprises a nickel silicide (see column 6, lines 6-15); **(15)** wherein said blocking layer has a thickness ranging from about 15nm to about 75nm (10 nm to about 35 nm) (see column 5, lines 3-5); **(17)** wherein said protective layer is a silicon nitride protective layer (see column 4, lines 13-17). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the MOS transistors of Kim and Pelella (accordance with the teaching of Wieczorek) and it also has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art and it is noted that the applicant does not disclose criticality in the ranges claimed. In re Aller, 105 USPQ 233 (see MPEP j 2144.05). Doing so would facilitate the manufacture of the semiconductor MOS transistor and increase the speed of the semiconductor device.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.



Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'C. Luu', with a stylized flourish at the end.

Chuong Anh Luu  
Patent Examiner  
November 16, 2005